DETAILED ACTION

Response to Arguments

Upon consideration of Applicant's remarks (5/11/2007) regarding the double patenting rejection on the record, as well as the amendments made herein, Examiner withdraws the Double patenting rejection which was previously set forth. Specifically, Applicants argued that in the '783 patent, the data is not limited to being transferred only one time to the bus, where in the present application only allows the byte to transit through the data bus from the first memory to the second memory once. Furthermore, Applicants note that in the '783 patent "the number of times one byte of the data element is transferred on the data bus is random" (see page 1 of the remarks files 5/11/2007) whereas in the instant application, a parameter of the transfer rule is randomly selected and, once again, each byte may transit once and only once through the data bus from the first memory to the second. Finally, the changes made to the claims for the Examiner's Amendment shown below now state that the bits within each byte (i.e. stream of data) remain unchanged when the transfer rule defines the order of how the bytes are to be transmitted via the data bus from the first memory to the second memory. For these reasons, Examiner has withdrawn the Double Patenting Rejection that was previously on record.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Bongini on May 6, 2008.

Please amend the application as follows:

Claims 1, 14, 22, and 25-26 should be amended to the claim language as shown below. These amended claims will **replace** claims 1, 14, and 22 as filed on 8/7/2006:

In claim 1, the amendment filed on 8/7/2006 **has been changed to** --A method for secured transfer through a data bus that is connected between a first memory and a second memory, said method comprising the steps of**:**

providing an N-byte data element in the first memory, wherein N has a value greater than 1;

randomly choosing the value of at least one parameter of a transfer rule before a transfer of the N-byte data element, the transfer rule defining the order in which the bytes of the N-byte data element are successively transferred through the data bus from the first memory to the second memory, without changing the order of the bits in that byte; and

successively transferring the N bytes of the data element byte-by-byte through the data bus to the second memory in the order specified by the transfer rule, with each of the N bytes transiting once and only once through the data bus.--

In claim 14, the amendment filed on 8/7/2006 **has been changed to** --A machine-readable medium encoded with a program for secured transfer through a data bus that is connected between a first memory and a second memory, said program containing instructions for performing the steps of**:**

providing an N-byte data element in the first memory, wherein N has a value greater than 1;

randomly choosing the value of at least one parameter of a transfer rule before a transfer of the N-byte data element, the transfer rule defining the order in which the bytes of the N-byte data element are successively transferred through the data bus from the first memory to the second memory, without changing the order of the bits in that byte; and

successively transferring the N bytes of the data element byte-by-byte through the data bus to the second memory in the order specified by the transfer rule, with each of the N bytes transiting once and only once through the data bus.--

In claim 22, the amendment filed on 8/7/2006 **has been changed to** --A programmable circuit comprising**:**

a data bus;

a read-only memory containing an N-byte data element to be transferred, the read only memory being coupled to the data bus and in the N-byte data element, N having a value greater than 1;

a writable memory coupled to the data bus;

a control unit coupled to the read-only memory and the writeable memory; and

a random number generator coupled to the control unit, the random number generator supplying the value of at least one parameter of a data transfer rule before a transfer of the N-byte data element from the read-only memory to the writable memory, the data transfer rule defining the order in which the bytes of the N-byte data element are successively transferred

through the data bus from the first memory to the second memory, without changing the order of the bits in that byte;

wherein the control unit controls the data bus such that the N bytes of the data elements are successively transferred byte-by-byte through the data bus to the writeable memory in the order specified by the transfer rule, with each of the N bytes transiting once and only once through the data bus.--

Claim 25 **has been cancelled**.

Claim 26 **has been cancelled**.

Allowable Subject Matter

Claims 1-7, 9-14, 16-17, 19-22, 24, and 27-28 are allowed.

The following is an examiner's statement of reasons for allowance: The above mentioned claims are allowable over the prior arts because the CPA (Cited Prior Arts) of record taken singly or in combination fail to anticipate or render obvious the specific added limitations, as recited in independent claims 1, 14, & 22 and subsequent dependent claims.

The CPA does not teach or suggest a method of transferring N data bytes, where N has a value greater than one, where a parameter of a transfer rule is randomly selected. Furthermore the CPA doesn't teach a particular transfer rule which defines the order that each byte will transit through the data bus from the first memory to the second memory without changing the order of the bits when the order of the bytes is to be determined. Finally, the CPA fails to suggest that each byte may transit one time, and one time only, through the data bus from the first memory to

the second memory as claimed (i.e. without chaining the bits from the byte that has transgressed to the byte that is to be transferred next as defined by the transfer rule).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadia Khoshnoodi whose telephone number is (571) 272-3825. The examiner can normally be reached on M-F: 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571) 272-3865. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

/Nadia Khoshnoodi/
Examiner, Art Unit 2137
5/6/2008

NK

/Emmanuel L. Moise/
Supervisory Patent Examiner, Art Unit 2137